Extended frequency-band-decomposition sigma–delta A/D converter

Philippe Benabes, Ali Beydoun, Jacques Oksman

Analog Integr Circ Sig Process (2009) 61:75–85
DOI 10.1007/s10470-008-9274-6

Extended frequency-band-decomposition sigma–delta A/D converter

Philippe Benabes · Ali Beydoun · Jacques Oksman

Received: 31 January 2008 / Revised: 5 December 2008 / Accepted: 9 December 2008 / Published online: 9 January 2009

Abstract Parallelism can be used to increase the bandwidths of ADC converters based on sigma–delta modulators. Each modulator converts a part of the input signal band and is followed by a digital filter. Unfortunately, solutions using bandpass sigma–delta modulators are very sensitive to the position of the modulators' central frequencies. This paper shows the feasibility of a frequency-band-decomposition (FBD) ADC using continuous time bandpass sigma–delta modulators, even in the case of large analog mismatches. The major benefit of such a solution, called extended-frequency-band-decomposition (EFBD) is its low sensitivity to analog parameters. For example, a relative error in the central frequencies of 4% can be accepted without significant degradation in the performance (other published FBD ADCs require a precision of the central frequencies better than 0.1%). This paper will focus on the performance which can be reached with this system, and the architecture of the digital part. The quantization of coefficients and operators will be addressed. It will be shown that a 14 bit resolution can be theoretically reached using 10 sixth-order bandpass modulators at a sampling frequency of 800 MHz which results in a bandwidth of 80 MHz centered around 200 MHz (the resolution depends on the effective quality factor of the filters of the analog modulators).

P. Benabes (✉) · A. Beydoun
SSE Department, SUPELEC, 3 rue Joliot Curie,
91192 Gif/Yvette, France
e-mail: philippe.benabes@supelec.fr

J. Oksman
Research Direction, SUPELEC, 3 rue Joliot Curie,
91192 Gif/Yvette, France
e-mail: Jacques.oksman@suplec.fr

Keywords Sigma–delta · Bandpass · Analog-to-digital conversion · Filter bank · Frequency-band-decomposition

1 Introduction

The current trend in telecommunication is high data rates, versatility and interoperability between digital mobile systems. Direct digitization of the input signal can simplify channel filtering, demodulation, or even channel detection but the bandwidth of the analog-to-digital converter must be enlarged.

Sigma–delta converters [1] are very good candidates to achieve high resolution conversion but the resolution decreases dramatically when the bandwidth increases.

Parallelism being a solution to increase the bandwidths without degrading the performance, solutions such as Time Interleaved sigma–delta (TIΣΔ)) [2], Parallel sigma–delta (ΠΣΔ) [3] and frequency-band-decomposition (FBD) [4], [5] have been proposed to widen the band of operation of the converters. The three solutions are compared in [6].

The TIΣΔ solutions (TI and random TI) have the lowest hardware complexity, but they have two main drawbacks: first, the whole frequency band between 0 and $F_s/2$ is converted, F_s being the sampling frequency, whereas the useful signal band may be lower. Moreover, the TI solutions are very sensitive to both offset and gain mismatches which leads to distortion and unwanted tones.

The FBD is the most natural way to widen the bandwidth of sigma–delta converters by using N parallel bandpass modulators, where each modulator processes a part of the input signal band. Thus the $1/f$ noise does not interfere and the front end of the converter is simplified. Furthermore, analog mismatches may result in distortion of

the signal transfer function (STF) but do not have non-linear effects.

The main issue of the solution proposed by Aziz in [4, 5] is its high sensitivity to the central frequencies of the bandpass modulators. Continuous-time (CT) modulators are the only way to process signals at very high frequencies but are not compatible with the precision required for the central frequencies of the modulators. Calibration of the analog part can be performed in the case of discrete-time modulators [7], but it is more complex in the case of continuous-time modulators, as it can induce non-linearities in their filters.

Finding a proper solution for these two problems is the main goal of this paper. In order to deal with analog mismatches (caused by variations in the manufacturing processes), two extra modulators, just outside the relevant signal band, are first used (Fig. 1). As a result, even if the central frequencies of the modulators are translated because of technology mismatches, the useful band may remain within the work band of the bank of modulators. A rough calibration of the analog part can be performed if technology process mismatches are too large.

Secondly, the digital processing is adapted to the fine characteristics of the analog modulators. This leads to a minimum quantization noise and allows for the reconstruction of the input signal by a transfer function as close as possible to a simple delay (minimum in-band ripple and linear phase). We call this solution extended frequency-band-decomposition (EFBD).

As in many conversion systems, a calibration of the digital part of the EFBD becomes unavoidable. The calibration proposed in [8] for FBD can only deal with offset and gain, which is not sufficient for EFBD solutions. The tuning of the digital part of EFBD will be one of the topics of this paper.

In Sect. 2, the performance of an FBD is predicted and a digital processing for the reconstruction of the input signal is proposed. The digital resources required for real-time conversion are also evaluated. Section 3 deals with the tuning of the digital processing in a non-ideal case. Simulation results of an EFBD using $8 + 2$ sixth order modulators will validate the feasibility of the EFBD principle in Sect. 4. Finally, the last section concludes with the perspectives of EFBD.

2 FBD design

2.1 FBD architecture

Parallel sigma–delta modulators [4, 5] are good candidates to convert signals with bandwidths higher than the limits of the technology since the input signal is processed simultaneously by multiple analog modulators as described in Fig. 2 (part A). Each modulator processes a part of the input signal band. The outputs of all channels are combined using a digital system (part B) to reconstruct the input signal. The oversampling ratio (OSR) of each modulator is equal to N times the OSR of the system, defined as $OSR_{sys} = F_s/2B$, F_s being the sampling frequency, B the bandwidth of the useful signal, and N the number of modulators. The order (Ord) of the modulator is defined as the order of its filter, i.e. in the bandpass case, twice the number of resonators ($Ord = 2m$).

Continuous-time modulators [9] (Fig. 2, part A) are used to overcome issues such as frequency limitation of the switched-capacitor circuits [10].

It is practically impossible to design continuous-time resonators with high quality factors (Q factors). The Q factors are limited by the serial resistor of the inductance [11] when the resonators are designed using passive LC tanks. They are limited by the output impedance of the amplifiers and by the parasitic elements when the resonators are designed with active elements such as Gm–C structures [12]. Active compensation can increase slightly the Q factor [13, 14] but may lead to instability. As a consequence, the Q factors of the resonators limit the performance of bandpass CT modulators. The Q factors

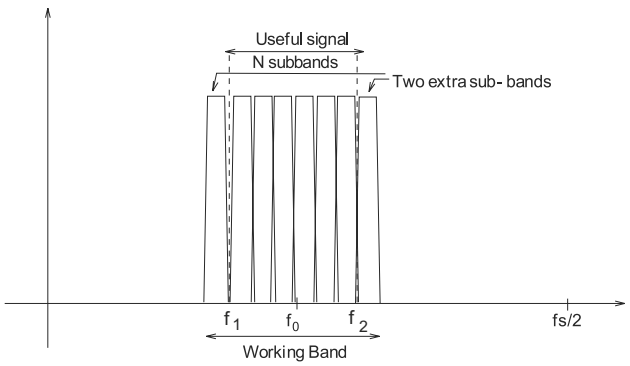

Fig. 1 Decomposition of the input signal band

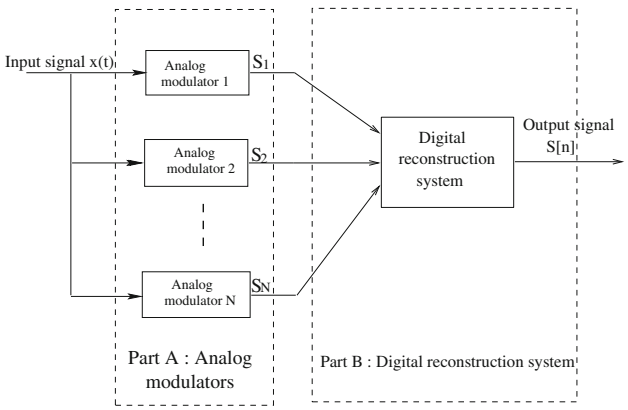

Fig. 2 Frequency band decomposition architecture

will be taken into account in the calculation of the FBD performance.

2.2 Expected performance

In this first approach, all modulators are supposed to be ideal with the exception of the finite Q factor of the filters. From now on, 6th order modulators with 3 resonators will be considered. They represent a good compromise between performance and stability and allow for innovative topologies [15, 16]. The input signal of the FBD is supposed to be band-limited between F_1 and F_2. The reduced frequencies (in lower case) are $f_1 = F_1/F_s$, $f_2 = F_2/F_s$. If Q factors are infinite, the best solution is reached when the modulators are uniformly spaced within the band [17]. Each modulator k should ideally process the subband k: $[f_A^k,...f_B^k]$, f_C^k being the center of subband k and Δf_k its half width, with:

$$\begin{cases} f_A^k = f_1 + (k-1)(f_2 - f_1)/N \\ f_B^k = f_1 + k(f_2 - f_1)/N \\ f_C^k = (f_A^k + f_B^k)/2 \\ \Delta f_k = (f_B^k - f_A^k)/2 \end{cases} \quad (1)$$

These results still represent a good approximation, even for non-infinite Q factors. The expected resolution can be estimated by calculating the output quantization noise power in each modulator. The total noise power at the output is the sum of all modulator noise power contributions: $P_{NTF_t} = \sum_{k=1}^{N} P_{NTF^k}$ (quantization noise of all modulators are supposed uncorrelated).

If the digital reconstruction system is supposed ideal, the quantization noise of each modulator is the contribution of the total noise in its subband.

$$P_{NTF^k} = \int_{f=f_A^k}^{f_B^k} \left|NTF^k(e^{2j\pi f})\right|^2 \Gamma_k(f) df \quad (2)$$

NTF^k is the noise transfer function of the kth modulator, $\Gamma_k(f)$ is the power spectral density of the quantization noise, and can be assumed constant under some hypotheses [18],

$$\Gamma_k(f) = \Gamma = \frac{1}{3 \times 4^{N_{bit}}}, \quad (3)$$

where N_{bit} is the number of bits of the ADC within the sigma–delta modulator. This model is most of the time relevant when multibit ADC and DAC are used. In the rest of this paper, three bit (eight level) ADC and DAC will be considered. This number of bits is large enough to justify the necessary "white noise additive assumption". Non-linearity issues may be solved by dynamic element matching algorithms [19].

Using the methodology based on the MSCL topology [20], the noise transfer function $NTF^k(z)$ of the $(2m)$th order modulator that is in the (k)th channel can be written as the product of m 2nd order noise transfer functions:

$$NTF^k(z) = \prod_{l=1}^{m} NTF_l^k(z) \quad (4)$$

By making a Taylor series expansion, each term in this equation can be approximated, for each modulator by (5) [17].

$$\left|NTF_l^k(e^{2j\pi f})\right|^2 \approx \frac{16\pi^2}{(c_l^k)^2}(f - f_l^k)^2 + \left(\frac{2\pi f_l^k}{Q_l^k c_l^k}\right)^2 \quad (5)$$

Coefficients c_l^k in (5) are linked to the gain of the resonators. The higher the c_l^k, the better the precision but the lower the gain margin of the loop.

The NTF of a bandpass sigma–delta modulator depends on the central frequencies f_l^k of its filters. Such frequencies should be chosen to minimize the in-band quantization noise (2). As $\Gamma_k(f)$ in (2) can be assimilated to a constant Γ, the noise power is proportional to the value defined below (6), that should be minimized.

$$P_{NTF^k} = \Gamma \int_{f_A^k = f_C^k - \Delta f_k}^{f_B^k = f_C^k + \Delta f_k} \left|\prod_{l=1}^{m} NTF_l^k(e^{2j\pi f})\right|^2 df \quad (6)$$

P_{NTF^k} will be minimum when the partial derivatives are null. For a 6th order modulator:

$$\left\{\frac{\partial P_{NTF^k}}{\partial f_1^k} = 0, \frac{\partial P_{NTF^k}}{\partial f_2^k} = 0, \frac{\partial P_{NTF^k}}{\partial f_3^k} = 0\right\} \quad (7)$$

The optimum resonance frequencies of the kth modulator can be obtained by solving Eq. 7. Assuming that all the Q factors and coefficients c_l^k are equal, that Δf_k is small, (7) has two sets of solutions expressed as (8):

$$\begin{aligned} f_1^k &= f_C^k - \lambda_k \cdot \Delta f_k \\ f_2^k &= f_C^k \\ f_3^k &= f_C^k + \lambda_k \cdot \Delta f_k. \end{aligned} \quad (8)$$

with either $\lambda_k = 0$ or $\lambda_k = \sqrt{\frac{3}{5}}\sqrt{\frac{1 - \frac{5\alpha_k^4}{\Delta f_k^4}}{1 + 3\frac{\alpha_k^2}{\Delta f_k^2}}}$ where $\alpha_k = \frac{f_C^k}{2Q^k}$.

For high enough Q factors $\left(1 - \frac{5\alpha_k^4}{\Delta f_k^4} > 0\right)$, the global minimum is found with the second solution, which is an improvement of the already published value $\left(\lambda_k = \sqrt{\frac{3}{5}}\right)$ in [21], and P_{NTF_k} becomes:

$$P_{NTF^k} = \Gamma\left(\frac{4\pi}{c}\right)^6 8\Delta f_k \left[\frac{\left(\alpha_k^6 + \Delta f_k^2 \alpha_k^4 + \frac{9}{35}\Delta f_k^4 \alpha_k^2 + \frac{1}{175}\Delta f_k^6\right)}{1 + \frac{3\alpha_k^2}{\Delta f_k^2}}\right] \quad (9)$$

The equivalent resolution can be obtained from (9) by using (2), (3) and the classical 6 dB/bit rule:

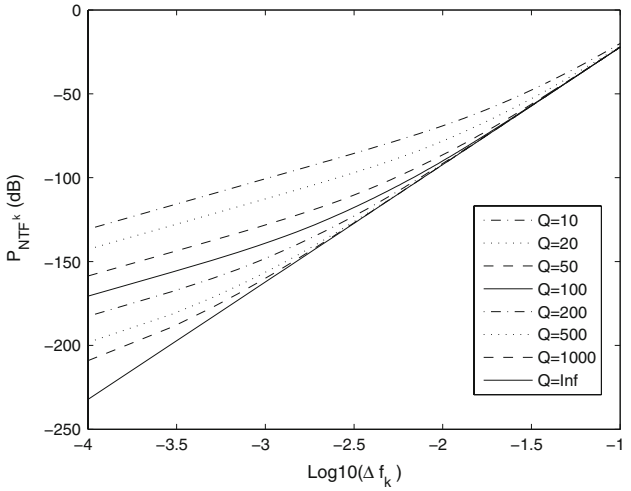

Fig. 3 P_{NTF} as a function of Δf for different values of Q with $f_C^k = 1/4$ and $c = 1/2$

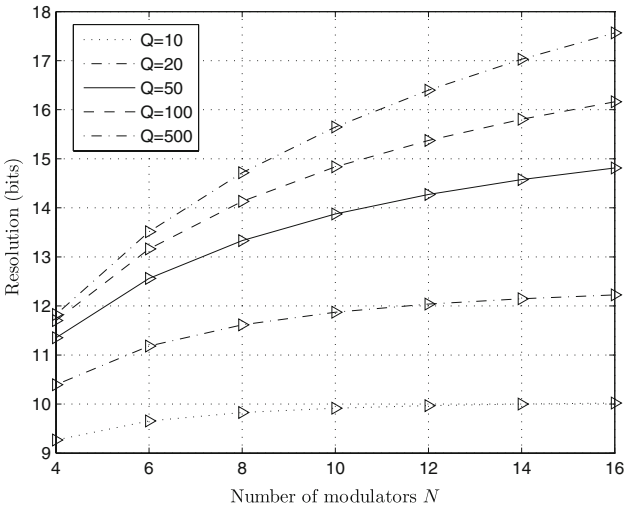

Fig. 4 Resolution as a function of N for different values of Q with $c = 1/2$

$$\text{Resolution} = N_{bit} - \frac{\log(P_{NTF^k}/\Gamma)}{\log(4)} \tag{10}$$

Figure 3 gives the value of P_{NTF^k} as a function of Δf_k for different values of Q. It can be noticed that for large Δf_k, Q factors have a weaker influence on the performances. The resolution of a single modulator can be estimated from (9) and (10). As the quantization noises of the modulators are not correlated, the global noise power is the sum of the noise power of each modulator. This leads to a loss of 1 bit for 4 modulators (noise power multiplied by 4) and 1.5 bits for eight modulators (noise power multiplied by 8). Finally, Fig. 4 gives the expected resolution of a FBD as a function of the number of modulators for different values of Q.

2.3 Digital reconstruction

The goals of the digital part of the FBD are:

- reconstruct the output signal with both, a minimum in-band ripple, and a minimum phase distortion,
- minimize the global quantization noise.

It was shown in [22] that a digital demodulation followed by a lowpass filter and modulation (Fig. 5) has a better performance than a direct processing using bandpass filters with the same number of filter coefficients. In this solution, the output of each channel is digitally demodulated by being multiplied by the complex sequence $m_k[n] = e^{2j\pi f_C^k n}$. The resulting signal is a complex baseband signal. We see that, if the central frequency can be expressed as a rational number, i.e. $f_C^k = p/q$ with p and q integer numbers, the sequence is periodic with period q. This will be useful in practical implementation, since this sequence can be pre-calculated and stored in a ROM.

Because of the previous oversampling by the modulators, the output must be decimated. The decimation can be achieved using classical comb filters [23]. Each signal is then processed by a lowpass filter before being remodulated (multiplication by the sequence $m'_k[n] = e^{2j\pi f_C^k N_d n}$) and added to the signals of the other channels. In our example the decimation factor is 5 ($\lceil OSR_{sys} \rceil$) resulting in an output frequency $F'_s = F_s/5$.

The choice of the window used for the low-pass filter influences the performance of the reconstruction and, particularly, the residual noise outside the band. Time domain simulations have shown that the Hann window gives the best results [22].

Table 1 gives the precision loss as a function of the number of coefficients of the lowpass filter, obtained by simulations.

It is worth mentioning that increasing the number of coefficients higher than 96 does not improve the resolution.

Figure 6 represents the frequency response (after modulation) of the eight lowpass filters (64 tap filters), and their sum. This sum shows a very low ripple (10^{-3}) within the frequency band, attenuations on the edges are as high as 6 dB. Note that the initial band ($[0.2F_s, 0.3F_s]$) has become $[0, F'_s/2\ ]$ due to the decimation by a factor 5.

2.4 STF flattening and phase alignment

The STF of a continuous-time ΣΔ modulator is not a simple time-delay transfer function as in discrete-time modulators. Furthermore, the frequency response of the decimation block that precedes the lowpass filters is not exactly flat and has some phase delay. Consequently an STF correction and a phase alignment between adjacent bands have to be performed, in order to minimize the

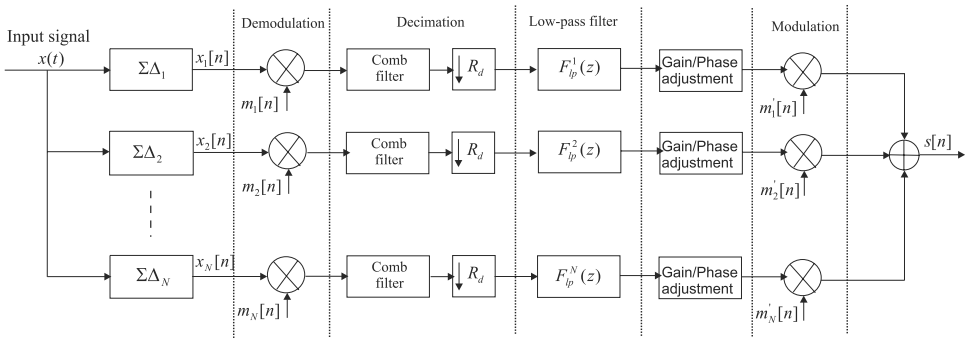

Fig. 5 Digital processing with demodulation

Table 1 Resolution loss with Hann window

Number of coefficients	48	56	64	96	128	256
Resolution loss (*bits*), *Hamming*	−1.17	−0.64	−0.04	0.05	0.06	0.05
Resolution loss (*bits*), *Blackman*	−0.46	−0.28	−0.15	0.03	0.08	0.07
Resolution loss (*bits*), *Hann*	−0.22	−0.12	−0.04	0.06	0.08	0.05

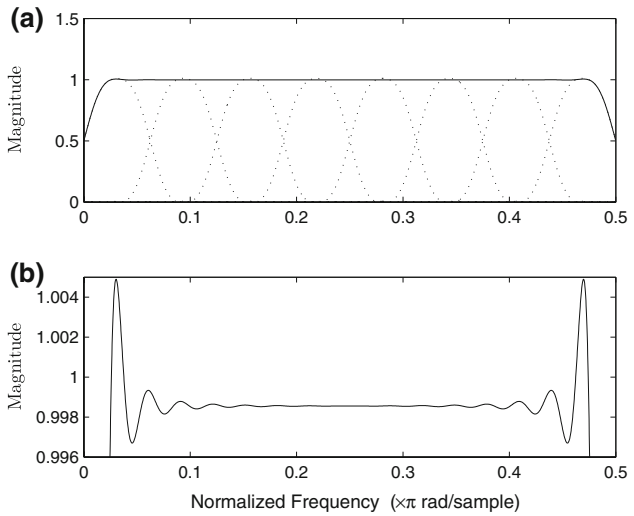

Fig. 6 Frequency response for eight 64 taps Hann FIR filters in the band (**a**) and a zoom on the ripples (**b**). (dotted lines are the responses of individual filters, and continuous line is the response of the sum of the filters)

ripples in the global STF. This correction will be divided into four steps:

- flattening the STF of the analog modulators,
- flattening the STF of the decimation filters,
- alignment of the phases of the analog modulators,
- alignment of the phases of the digital filters.

2.4.1 Flattening the STF of the analog modulators

The STF of each modulator is not flat in the band, but usually presents approximately a parabolic form. The center of the parabola is usually not centered in the band-pass of the modulator [24]. A correction filter must be applied to flatten the STF.

This correction filter must be applied to the decimated signal because of its lower rate. Assuming a 2nd order polynomial approximation of the modulator's STF in the relevant band, the flattening factor in the Z domain can be expressed as:

$$C_1(z) = \left(-\varepsilon e^{-2j\pi\varphi} + (1+2\varepsilon)z^{-1} - \varepsilon e^{2j\pi\varphi} z^{-2}\right) g \tag{11}$$

where ε is the curvature of the parabola, φ the difference between the center of the subband and the frequency for which the STF is maximum, and g the inverse of the maximum of the STF magnitude.

2.4.2 Flattening the amplitude of decimation filters

The comb filters used for the decimation [23] can be expressed as:

$$C(z) = \left(\frac{1 - z^{-N_d}}{N_d(1 - z^{-1})}\right)^r, \tag{12}$$

with $r \geq Ord/2 + 1$, N_d: decimation factor.

The frequency response of this filters is given by:

$$\left|C(e^{2j\pi f})\right| = \left|\frac{\sin(N_d \pi f)}{N_d \sin(\pi f)}\right|^r \tag{13}$$

In order to correct the transfer function of this filter, a 3-coefficient correction filter (after the decimation) is added (14).

$$C_2(z) = -\varepsilon + (1 - 2\varepsilon)z^{-1} - \varepsilon z^{-2} \tag{14}$$

The calculation of ε is made by identifying the second order term of the Taylor series expansions of (13) and $\left|C_2(e^{2j\pi f})\right|$:

$$\varepsilon = \frac{\left(1 - \frac{1}{N_d^2}\right) r}{24} \tag{15}$$

2.4.3 Alignment of the phases of the analog modulators

The sigma–delta converters have an almost linear phase around their central frequency (Fig. 7(a)). However, their

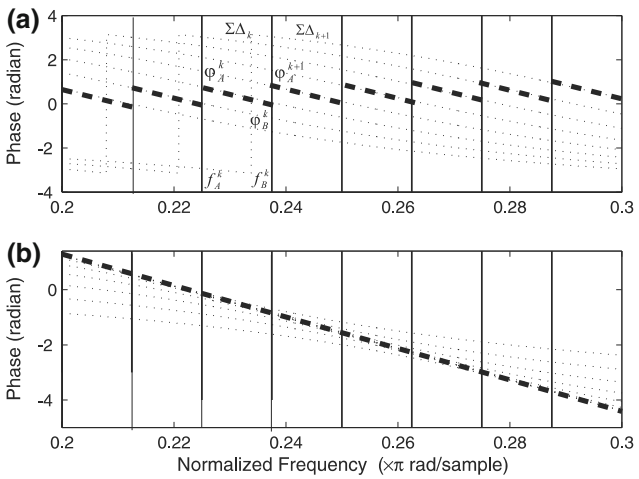

Fig. 7 Sigma–delta phases before (**a**) and after alignment (**b**)

phases are not continuous in the transition zone between adjacent subbands. This phase discrepancy can be compensated by multiplying the signal in each channel with a constant factor in order to obtain a continuous phase in the full band (Fig. 7(b)). The value of this correction can be calculated as follows:

ϕ_A^k and ϕ_B^k are the phases of the signal transfer function of modulator k at frequencies f_A^k and f_B^k. The corrective coefficient for the kth modulator ($k \geq 2$) must then be (Fig. 7):

$$C_3^k = e^{2j\pi \sum_{m=2}^{k} (\phi_A^m - \phi_B^{m-1})} \tag{16}$$

2.4.4 *Alignment of the phases of the digital filters*

All the filters used in the baseband, e.g. the decimation filter, corrective filters, and lowpass filter have a linear phase. Due to demodulation and remodulation, the signals in the transition zone between two adjacent channels are not in phase. A $2L + 1$ coefficients FIR filter introduces a phase lag $\tau_1^k = 2\pi(f_B^k - f_C^k)L$ at frequency f_B^k for modulator k. The phase lag is $\tau_2^{k+1} = 2\pi(f_A^{k+1} - f_C^{k+1})L$ for modulator $k + 1$ at frequency f_A^{k+1}. As $f_B^k = f_A^{k+1}$, the phase alignment required between modulator k and modulator $k + 1$ is $\tau_2^{k+1} - \tau_1^k$. Thus the output of each channel k, when the filter is applied after the decimation, must be multiplied by the complex number:

$$C_4^k = e^{2j\pi(f_C^k - f_C^1)LN_d} \tag{17}$$

This phase alignment has to be performed once for each modulator (decimation filter, lowpass filter, decimation correction, STF correction) since the global correction factor is the product of the four elementary corrections.

2.5 Implementation of the digital processing, computing resources

Practically, the amplitude correction of the decimation filter should be included in the low pass filter following the decimation filter (Fig. 5), as its coefficients are known and constant. The coefficients of the resulting filter are stored in a ROM. The modulator's STF correction filter has to be implemented separately since its coefficients depend on the characteristics of the analog modulators. All the phase alignment coefficients are multiplied and lead to a single factor included as a phase shift in the modulation sequence. The demodulation and modulation sequences can be precalculated assuming that the central frequencies of each subband and $\Phi_k/2\pi$ can be expressed as rational numbers. These sequences may be stored in a ROM.

The whole processing for one modulator is summarized in Fig. 8.

In order to be implemented in an ASIC, all coefficients of the digital filter should be quantized and represented using fixed-point arithmetic. It has been shown from simulation results (Fig. 9) [17] that an 11 bit FIR coefficients word length is a good compromise to reach the expected resolution

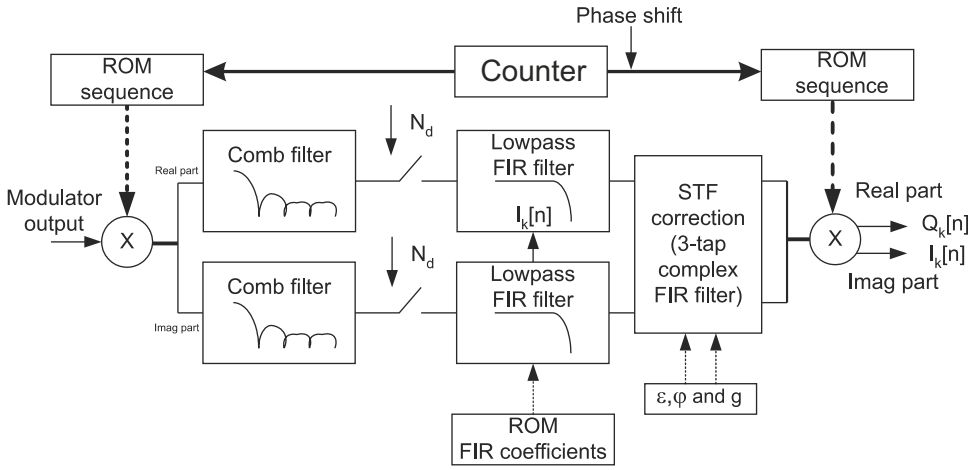

Fig. 8 Full processing for one modulator

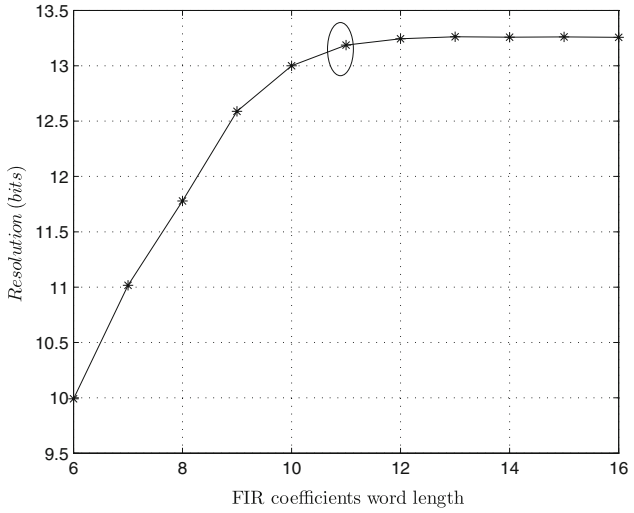

Fig. 9 Resolution as a function of FIR coefficients word length

about 13.3 bits. The modulation and demodulation sequence use also 11 bit word length as the bandwidth will be quantized with a step $q_s = 10^{-3}F_s$ (see Sect. 3.1).

The computing resources needed for one modulator are summarized in Table 2. The first three columns of the table give the number of multipliers and adders required for each function and the number of operations per second. The two last columns give the synthesis results of each function in a 0.12 µm CMOS digital technology in terms of flip flop number, gate number and area (mm^2). The synthesis has been performed from a VHDL model of each function. The FIR coefficients are quantized on 11 bits and the sine functions for the demodulation and modulation are coded on 11 bits. The ROMs have been replaced by spare logic (no ROM was available in the target technology).

The STF correction, modulation, and demodulation use less than 30% of the whole logic resources. Most of these resources are used by the comb and the FIR filters. It turns out that the digital processing power is approximately proportional to the converted bandwidth. This solution uses almost the same resources (in term of operations per second) as a solution using a single ΣΔ modulator running 8 times faster. The whole estimated area of the digital part for ten modulators would be 6 approximately mm^2.

Table 2 Computing resources for one modulator

	Multipliers	Adders ROM	Op/sec	FFD gates	Area (mm^2)
Demodulation	0	(N_{bit})*2	F_s	167 2.5 K	0.027
Comb filter	0	4*2	F_s	300*2	0.026*2
	0	4*2	F'_s	2.2 K*2	
Lowpass FIR filter	7*2	7*2	F'_s	1.8 K*2 15 K*2	0.2*2
STF correction	6	10	F'_s	914 3.4 K	0.07
Modulation	4	2	F'_s	550 4.9 K	0.07

The maximum clock frequency for each function in the used technology is 800 MHz. Higher sampling frequency such as 2 GHz will probably be reached using advanced 65 or 45 nm technologies.

3 Tuning the EFBD digital processing to non-ideal modulators

In Sect. 2, the analog modulators were supposed "ideal" where all the central frequencies of the resonators (f_1^k, f_2^k, f_3^k) were equal to their theoretical values. In this section, the digital processing deals with non-ideal values.

The main idea, as shown in Fig. 1, is to use two extra modulators, numbered '0' and '$N + 1$', one on each side of the relevant band. With this configuration the signal band remains within the work band of the converter, even if there is a reasonable mismatch on central frequencies.

For instance, in the present case, by adding two extra modulators, ($N = 8$ modulators and a band of interest between $F_1 = 0.2F_s$ and $F_2 = 0.3F_s$), an identical relative error on the central frequencies between -4% and $+6.66\%$ is allowed.

3.1 Digital filtering tuning

In this section, it is supposed that the central frequencies of the resonators are not at their typical values but are known. The band of each modulator, i.e. the boundaries between adjacent modulators, must be determined. The rule is to use for each frequency band the modulator that presents the lowest quantization noise density.

The frequency of the boundary between modulators k and $k + 1$ (f_r^{k+1}) is obtained by solving the Eq. 18.

$$\left|NTF^k(e^{2j\pi f_r^{k+1}})\right|^2 = \left|NTF^{k+1}(e^{2j\pi f_r^{k+1}})\right|^2 \quad (18)$$

The lower boundary of the first modulator (f_r^0) is always f_1, the higher boundary of the last modulator (f_r^{N+2}) is always f_2, and $f_r^k \le f_r^{k+1}$. When a modulator is not used, its boundaries are equal. The half bandwidth of the channel k is now defined as:

$$\Delta f_k = (f_r^{k+1} - f_r^k)/2, \quad (19)$$

and its central frequency:

$$f_C^k = (f_r^{k+1} + f_r^k)/2. \quad (20)$$

Figure 10, gives an example (10 modulators), where all resonator frequencies have been shifted upwards by half a

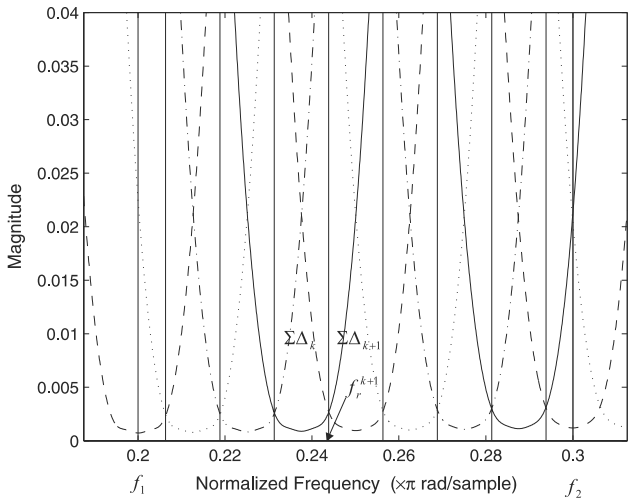

Fig. 10 Boundaries with non-ideal modulators

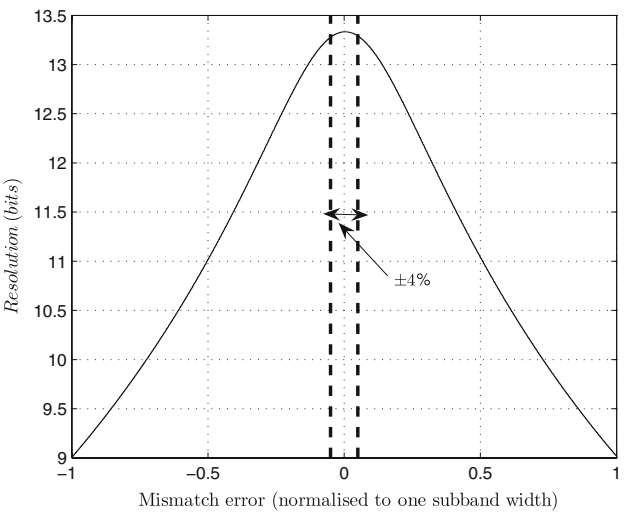

Fig. 11 Mismatch effect between the digital and the analog part

bandwidth. The ten curves are the magnitudes of the noise transfer function of the modulators (the Q factors have been chosen equal to the optimistic value of 25).

The bandwidths of the first and ninth modulators (0.00625) are half the bandwidth of the other modulators (0.0125). The tenth modulator is not used.

Four elements have to be adapted in order to fit the digital process and the analog part: the demodulator, the lowpass filter, the modulator, and the phase alignment block. The demodulation and modulation sequences use the new central frequencies f_C^k obtained from Eq. 20. The bandwidths of the lowpass filters are $\Delta f_k * N_d$, obtained from Eq. 19 and the filter phase alignment due to demodulation, still uses Eq. 17, now with the real values of the central frequencies of each subband.

The last parameter to workout is the accuracy with which the digital part must fit the parameters of the analog modulators. A mismatch between the frequencies of the modulators and the frequencies used by the digital part has been introduced. Figure 11 gives the precision function of this error (normalized to a subband width). An error of 4% on the width of the subband (0.05% of the sampling frequency) causes a resolution loss less than 0.1 bit. Thus, the boundary frequency values (f_r^k) can be quantized with a step $q_s = 10^{-3} F_s$. It results that even the analog part is non-ideal, the central frequency and the bandwidth of each subband is quantized and can be expressed as a rational number. The modulation and demodulation sequences remain finite and can still be stored in a ROM.

3.2 Computing resources

The computing resources required by an EFBD are almost the same as an FBD except that the number of effectively running modulators is usually increased by 1 (12.5% increase with 8 modulators). The FIR coefficients can be pre-calculated and stored in a ROM or downloaded from outside the digital processing chip. The number of possible widths is not very large. In the example used all along this paper, the width of each subband is nominally 0.0125 F_s. Even with large mismatches, one real subband will not be wider than twice the nominal value (0.025). The precision required for the digital part is 0.001 (Subsect. 3.1). Thus the FIR coefficients have to be calculated for 25 possible widths, resulting in a memory of 0.8 K words, which is quite small in today's technologies.

4 Simulation results

4.1 Simulation of an ideal EFBD

To illustrate the points raised above, an architecture with eight sixth-order modulators simulated with a wide band input signal is given as an example. The quality factors of the modulators have been chosen equal to 50. The input signal is a cardinal sine, has a limited band of 80 MHz centered around 200 MHz and is sampled at $F_s =$ 800 MHz. The theoretical resolution obtained with a 64-tap Hann FIR filter is around 13.3 bits.

Figure 12 represents the power spectral densities of the input signal, the output signal, and the output noise. There is a slight difference on the edges of the power spectral densities between the input signal and the output signal. This is related to the fact that the sum of the responses of the lowpass filters is attenuated on their edges (Fig. 6).

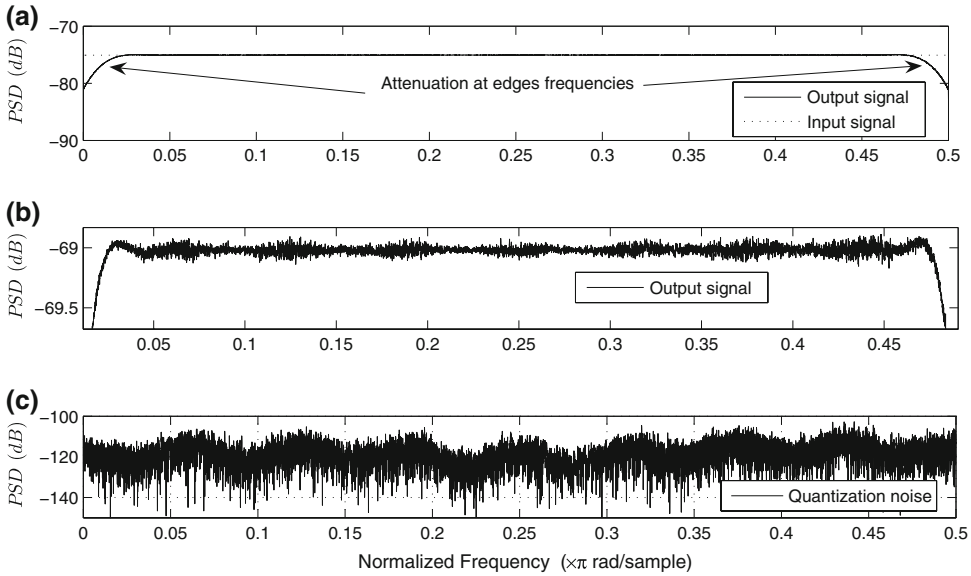

Fig. 12 Power spectral density for input signal (**a**), output signal (**b**) and quantization noise (**c**)

4.2 Effect of non-idealities

This section focuses on the impact of the non-idealities on the expected performance. In a first part, the case of a shift of the central frequencies of all filters by the same constant value is pointed out. Figure 13 shows the impact of this shift on the performance of the converter (a value of 1 is the width of one subband) without and with calibration. It may be seen that, as expected, a shift lower than one subband does not affect the performance of the EFBD whereas the same shift without calibration would cause a loss higher than 4 bits.

Unfortunately, the real case is far from ideal. The main reason for the central frequencies value errors is technology mismatch. It can be modelled by a roughly constant factor in all central frequencies. Figure 14 shows the impact of this multiplication on the performance of the converter (the value of the *X*-axis is the real multiplicative factor). Each resonator central frequency for each modulator has been multiplied by the same coefficient (*X*-axis). When the system is calibrated, this shift has a small impact (it can even improve the performance if this factor is lower than one). By limiting the error to 5%, the precision loss is lower than 0.1 bit whereas the same shift without calibration would cause a loss of more than 5 bits.

The second error is due, in the case of integrated circuits, to local mismatches and to the quantization of the sizes of transistors and passive elements. These sizes must

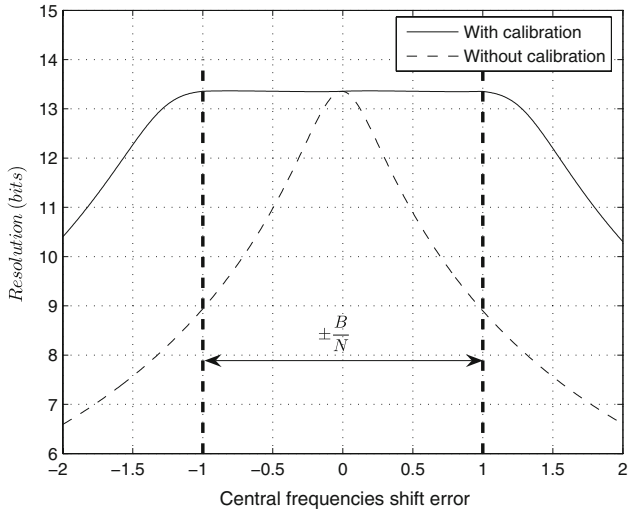

Fig. 13 Effect of a frequency shift on the performance

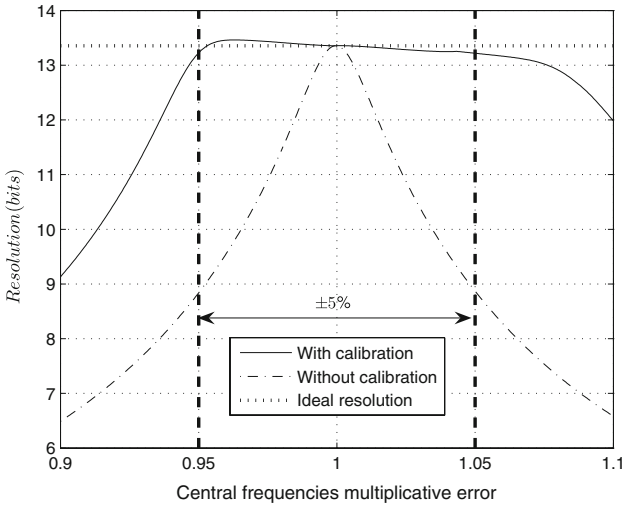

Fig. 14 Effect of a frequency multiplication on the performance

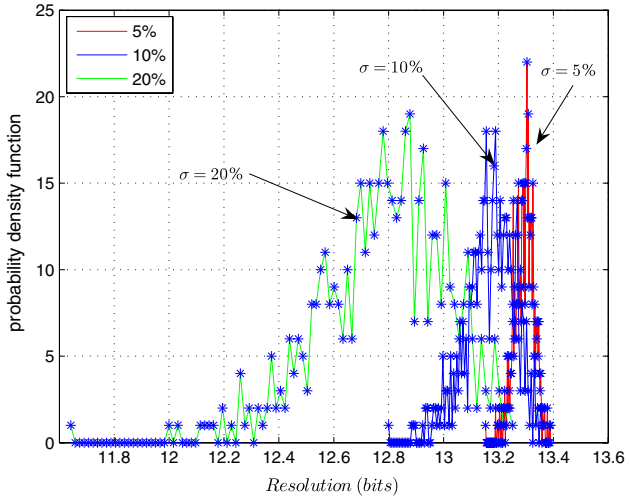

Fig. 15 Histogram of resolution for 5%, 10% and 20% standard deviation

be a multiple of a unit step. The size errors and local mismatches lead to random losses. Some Monte Carlo simulations have been performed. All frequencies have been multiplied by 1.01 (1% error due to technology shift) and each central frequency has been affected by a gaussian random error. Some simulations with standard deviations σ of 5%, 10%, and 20% of one subband bandwidth (relative errors of 0.25% 0.5% and 1% for $f_C^k = 1/4$) have been performed. Mismatch errors of 1% (Fig. 15) may reduce the performance of 0.5 bit with a standard deviation less than 0.3 bit, which is quite acceptable.

5 Conclusion

This paper shows that the proposed architecture permits the conversion of wideband signals, considering the obtained performance, namely a bandwidth of the tenth of the sampling frequency with a precision of 13.3 bits, using CT modulators with realistic Q factors equal to 50. The computing power and chip area (6 mm^2) with an up-to-date technology (0.12 µm) are reasonable values. Sensitivity to analog mismatch can be reduced to a value compatible with an implementation with classical technology. Indeed, we show that an error of 4% in the characteristics of the central frequencies of the modulators can be allowed without performance degradation as long as the digital part is correctly matched to the analog modulators. Fitting the digital part to the analog modulators consists in changing coefficients used for modulation, demodulation and FIR filtering, and does not require extra computing resources (except for the calibration phase). The present assumption of prior matching between analog and digital parts can be removed by the use of self calibration methods. These methods are not the scope of this paper, but simple algorithms such as relaxation algorithms have been tested, resulting in a realistic calibration scheme.

References

1. Schreier, R., & Temes, G. C. (2005). *Understanding delta–sigma data converters*. New Jersey: Wiley, chap. 4.
2. Eshraghi, A., & Fiez, T. (2003). A time-interleaved parallel ΔΣ A/D converter. *IEEE Transactions on Circuits and Systems II, 50*, 118–129.
3. Galton, I., & Jensen, H. T. (1995). Delta–sigma modulator based A/D conversion without oversampling. *IEEE Transactions on Circuits and Systems II, 42*(12), 773–784.
4. Aziz, P., Sorensen, H., & Van der Spiegel, J. (1993). Multiband sigma–delta modulation. *Electronics Letters, 29*(9), 760–762.
5. Aziz, P., Sorensen, H., & Van der Spiegel, J. (1994). Multiband sigma–delta analog to digital conversion. In *Proceedings of ICASSP' 1994*, April 1994, Vol. 3, pp. 249–252.
6. Eshraghi, A., & Fiez, T. (2004). A comparative analysis of parallel delta–sigma ADC architectures. *IEEE Transactions on Circuits and Systems I, 51*, 450–458.
7. Gandolfi, G., Colonna, V., Annovazzi, M., Stefani, F., & Baschirotto, A. (2004). Self-tuning algorithms for high-performance bandpass switched-capacitor ΣΔ modulators. *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications, 51*, 170–174.
8. Batten, R. D., Eshraghi, A., & Fiez, T. S. (2002). Calibration of parallel ΣΔ ADCs. *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing, 49*, 390–399.
9. Benabes, P., Keramat, M., & Kielbasa, R. (1997). A methodology for designing continuous-time sigma–delta modulators. In *Proceedings of European Design and Test Conference*, March 1997 (pp. 46–50).
10. Ortmanns, M., & Gerfers, F. (2006). *Continuous-time sigma–delta A/D conversion*. Berlin: Springer.
11. Cherry, J. A., Snelgrove, W. M., & Gao, W. (2000). On the design of a fourth-order continuous-time LC delta–sigma modulator for UHF A/D conversion. *IEEE Transactions on Circuits and Systems II, 47*, 518–530.
12. Shoaei, O., & Snelgrove, W. M. (1994). Optimal (bandpass) continuous-time Σ−Δ modulator. In *Proceedings of IEEE International Symposium on Circuits and Systems*, Jun 1994 (Vol. 5, pp. 489–492).
13. Jayaraman, A., Asbeck, P., Nary, K., Beccue, S., & Wang, K. C. (1997). Bandpass delta–sigma modulator with 800 MHz center frequency. *IEEE Technical Digest, 19th Annual Gallium Arsenide Integrated Circuit (GaAs IC) Symposium*, March 1997 (pp. 95–98).
14. Gao, W., Asbeck, P., & Snelgrove, W. M. (1998). A 950 MHz IF second-order integrated LC bandpass delta–sigma modulator. *IEEE Solid-State Circuits, 33*, 723–732.
15. Lelandais-Perault, C., Benabes, P., De Gouy, J. L., & Kielbasa R. (2003). A parallel structure of a continuous-time filter for bandpass sigma–delta A/D converters. *10th IEEE International Conference on Electronics, Circuits and Systems*, December 2003 (pp. 14–17)
16. Benabid, S., Najafi-Aghdam, E., Benabes, P., Guessab, S., & Kielbasa, R. (2004). CMOS design of a multibit bandpass continuous-time sigma delta modulator running at 1.2 GHz. *IEEE*

International Caracas Conference on Devices, Circuits and Systems, November 2004 (pp. 51–55).
17. Beydoun, A. (2008). *Bandpass wideband parallel sigma–delta converters*. PhD Thesis, Department of Signal Processing and Electronic Systems, Supelec, France.
18. Bennett, W. R. (1948). Spectra of quantized signals. *Bell System Technical Journal, 27*, 446–472.
19. Benabes, P., & Najafi-Aghdam, E. (2006). A hardware efficient 3-bit second-order dynamic element matching circuit clocked at 300 MHz. In *Proceedings of IEEE International Symposium on Circuits and Systems*, May 2006 (pp. 2977–2980).
20. Benabes, P., Gauthier, A., & Kielbasa R. (1996). A multistage Closed-Loop Sigma–Delta Modulator (MSCL). *Journal of Analog Integrated Circuits and Signal Processing, 11*(3), 195–204.
21. Schreier, R. (1993). An empirical study of high-order single-bit delta–sigma modulators. *IEEE Transactions on Circuits and Systems II, 40*, 461–466.
22. Beydoun, A., & Benabes P. (2006). Bandpass/wideband ADC architecture using parallel delta sigma modulators. In *Proceedings of the 14th European Signal Processing Conference*, September 2006, 1568981598.pdf.
23. Chu, S., & Burrus, C. S. (1984). Multirate filter design using comb filters. *IEEE Transactions on Circuits and Systems II, CAS-31*, 913–924.
24. Hussein, A. I., & Kuhn, W. B. (2000). Bandpass ΣΔ modulator employing undersampling of RF signals for wireless communication. *IEEE Transactions on Circuits and Systems II, CAS-47*, 614–620.

Philippe Benabes was born in NICE in 1967. He received the degree of "Diplôme d'Ingénieur de l'Ecole Centrale Paris" in 1989. From 1989 to 1991, he worked for Thomson Sintra ASM as a board designer. He received the Ph.D. degree in 1994 for the work "Wideband Bandpass SigmaDelta Converters". He is currently professor of electronics at Supélec and holds an "Habilitation à diriger les recherches". His research interests include both analog and digital electronics and particulary the design of bandpass sigma-delta analog-to-digital converters.

Ali Beydoun was born in Beirut, Lebanon, in 1980. He received a B.S. in Electronics from the University of Lebanon in 2002, an Engineering Degree in Telecommunications from the ENSIETA school, Brest, France, in 2004 and a M.Sc. degree in Technology and Telecommunication from the UBO University in 2004. He is currently pursuing a Ph.D. degree in high performance digitizing systems at the Department of Signal Processing and Electronics Systems, SUPELEC, Paris, France. His research focuses on the development of novel wideband analog to digital converter architectures, mostly in the field of parallelism of sigma-delta modulators.

Jacques Oksman was born in Toulouse, France, in 1948. He received an Engineering Degree from the Ecole Supérieure d'Electricité (Supélec) in 1971. He also holds an "Habilitation à diriger les recherches". He is currently Professor at Supélec and Director of Research and industry partnerships of Supélec. His main interests are Signal Processing for measurement purposes and non-uniformly sampled signals. He has been working on various research projects involving such topics as parametric modeling of signals, systems for solving inverse problems, real-time identification or prediction of non-uniformly sampled signals. He teaches courses on Digital Design, Numerical Analysis and Optimization.